IN THE CLAIMS

1.-4. (Canceled)

5. (Previously Presented) A bimodal power data link transceiver device, the device comprising:

a transceiver integrated circuit (IC), the transceiver IC comprising:

a transmitter, the transmitter having;

a phase locked loop (PLL) frequency synthesizer comprising a partial first voltage controlled oscillator (VCO);

a first power amplifier, the first power amplifier coupled to the PLL frequency synthesizer; and

a receiver;

a second power amplifier coupled to the first power amplifier;

a transmit/receive switch coupled to the second power amplifier and the receiver;

a controller coupled to the transceiver IC;

a direct digital frequency synthesizer having an output coupled to an input of the transceiver IC;

a second voltage controlled oscillator (VCO) coupled to the partial first VCO; and

a loop filter coupled to the second VCO and the transceiver IC.

6. (Previously Presented) A bimodal power data link transceiver device as in claim 5, wherein the PLL frequency synthesizer comprises:

a phase detector coupled to the loop filter; and

a crystal oscillator coupled to the phase detector.

7. (Original) A bimodal power data link transceiver device as in claim 5, wherein the receiver comprises:

a low noise amplifier;

a quadrature mixer pair, the quadrature mixer pair coupled to the low noise amplifier and the PLL frequency synthesizer, the quadrature mixer pair having:

a first quadrature signal;

a second quadrature signal;

a demodulator;

a first signal channel, the first signal channel coupling the first quadrature signal to the demodulator; and

a second signal channel, the second signal channel coupling the second quadrature signal to the demodulator.

8. (Original) A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC comprises at least one field programmable gate array (FPGA).

9. (Original) A bimodal power data link transceiver device as in claim 5 wherein the transmit/receive switch comprises a plurality of diodes.

10. (Currently Amended) A method for transceiving data in a device adapted to transceive data in the radio frequency spectrum, the method comprising:

providing a transceiver integrated circuit (IC), the transceiver IC having:

a partial first voltage controlled oscillator (VCO);

an oscillator input port coupled to the partial first VCO;

a frequency reference port;

a radio frequency input port;

a radio frequency output port;

a phase detector output port;

using a second VCO, generating a VCO signal for input to the oscillator input port;

coupling a direct digital synthesizer (DDS) to the frequency reference port;

coupling the radio frequency output port to a power amplifier; and

coupling the radio frequency input port to a transmit/receive switch.

11. (Previously Presented) A method as in claim 10 wherein providing a transceiver IC further comprises:

providing a field programmable gate array (FPGA);and

programming the FPGA to operate as a transceiver.

12. (Previously Presented) A method as in claim 10 wherein the step of generating a voltage controlled oscillator signal for input to the oscillator port further comprises;

coupling the phase detector output port to at least one loop filter; and

coupling the at least one loop filter to the second VCO.

13. (Previously Presented) A method as in claim 10 wherein coupling a DDS to the frequency reference port further comprises coupling a first microprocessor controller to the DDS.

14. (Previously Presented) A method as in claim 13 wherein coupling the first microprocessor controller to the DDS further comprises setting a center transmit frequency.

15. (Previously Presented) A method as in claim 13 wherein coupling the first microprocessor controller to the DDS further comprises modulating a transmit frequency.

16. (Previously Presented) A method as in claim 10 further comprising:

operating the device in a quiescent baseline receiver mode, wherein the quiescent baseline receiver mode comprises a first power mode;

operating the device in a burst transmit mode when not in the quiescent baseline receiver mode, wherein the burst transmit mode comprises a second power mode, wherein the second power mode is greater than the first power mode;

operating the device with a transmit/receive time ratio less than 1.5; and

transceiving a RF carrier frequency less than 200 MHz.

17. (Previously Presented) A method as in claim 10 further comprising operating the device with a global positioning indicator.

18. (Original) A method as in claim 10 further comprising transceiving data in weapons munitions, wherein transceiving data in weapons munitions further comprises transmitting frequency shift key (FSK) modulated signals.

19. (Original) A method as in claim 10 further comprising transceiving data in a landmine.

20. (Original) A bimodal power data link transceiver device, the device comprising:

a receiver section;

a transmitter section;

a phased locked loop (PLL) frequency generator section, wherein the PLL frequency generator section comprises:

a first voltage controlled oscillator (VCO);

an integrated circuit (IC), wherein the integrated circuit comprises:

a first buffer, wherein the buffer is coupled to the first VCO, the first buffer comprises:

a partial second VCO,

a digital direct synthesizer (DDS), wherein the DDS is coupled to the IC; and

a controller section, the controller section coupled to the PLL frequency generator section and the receiver section.

21. (Original) A bimodal power data link transceiver device as in claim 20, wherein the transmitter section comprises:

the IC, the IC further comprising:

a first amplifier, wherein the first amplifier is coupled to the PLL frequency generator section; and

a second amplifier, the second amplifier coupled to the first amplifier.

22. (Original) A bimodal power data link transceiver device as in claim 20, wherein the receiver section comprises:

a low noise amplifier;

a quadrature mixer pair coupled to the low noise amplifier; and

a demodulator coupled to the quadrature mixer pair.

23. (Original) A bimodal power data link transceiver device as in claim 20, wherein the device is adapted to fit in a weapon.

24. (Original) A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a landmine.

25. (Original) A bimodal power data link transceiver device as in claim 23 wherein the weapon comprises a sea mine.

26. (New) A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC is configured to operate at and above a first frequency and wherein the second VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency.

27. (New) A method as in claim 10, wherein the transceiver IC is configured to operate at and above a first frequency and wherein generating a VCO signal further comprising using the second VCO to generate the VCO signal at a second frequency at which the transceiver IC operates, the second frequency smaller than the first frequency.

28. (New) A bimodal power data link transceiver device as in claim 20, wherein the integrated circuit is configured to operate at and above a first frequency, wherein the first VCO is configured to operate the transceiver IC at a second frequency, and wherein the second frequency is smaller than the first frequency.

29. (New) A bimodal power data link transceiver device, the device comprising:

a transceiver integrated circuit (IC) configured to operate at and above a first frequency, the transceiver IC comprising:

a transmitter, the transmitter having:

a partial first voltage controlled oscillator (VCO);

a first power amplifier, the first power amplifier coupled to the partial first VCO; and

a receiver coupled to the partial first VCO,

a second power amplifier coupled to the first power amplifier;

a transmit/receive switch coupled to the second power amplifier and the receiver;

a controller coupled to the transceiver IC;

a direct digital frequency synthesizer coupled to the controller and having an output coupled to an input of the transceiver IC;

a second voltage controlled oscillator (VCO) coupled to the partial first VCO, wherein the second VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency; and

a loop filter coupled to the second VCO and the transceiver IC.

30. (New) The device of claim 29, wherein the partial VCO is configured to be one of an emitter follower, a buffer, or a filter.

31. (New) The device of claim 29, wherein the first frequency is 300 megahertz (MHz) and the second frequency is 200 MHz.

connected to a second VCO"). For ease of reference, the subject matter in independent claims 5, 10, and 20 the Examiner asserts is found in Iwasaki is referred to herein as the "Iwasaki subject matter". The rejections in (2)-(5), which are of claims dependent on claims 5, 10, and 20, use a combination of the BlueChip Manual and Hareyama and other references, but none of the rejections in (2)-(5) use Iwasaki and none of the references in rejections (2)-(5) appear to disclose the Iwasaki subject matter. Consequently, Applicants have assumed herein that the rejections in (2)-(5) are rejections based on a combination of the BlueChip Manual, Hareyama, and Iwasaki and the other references cited in each of (2)-(5). If this assumption is not correct, then the rejections in (2)-(5) do not disclose all elements of independent claims 5, 10, 20 as the Iwasaki subject matter is not found in the rejections of (2)-(5) and therefore dependent claims 8, 11, 13-17, 19, and 23-25 are patentable over the references cited in (2)-(5). Furthermore, if this assumption is not correct, Applicants respectfully request another non-final Office Action in order to respond appropriately to the rejections in claims (2)-(5).

With regard the rejections in (1) above and specifically to the rejections to independent claims 5, 10, and 20, each of these claims is partially directed to an integrated circuit (IC) having a partial voltage controlled oscillator (VCO) and another VCO, outside the IC, coupled to the partial VCO inside the IC. As described in more detail below, Applicants respectfully submit that the combination of the BlueChip Manual, Hareyama, and Iwasaki does not establish a *prima facie* case of obviousness.

When rejecting independent claim 1, the Examiner admits that the combination of BlueChip Manual and Hareyama does not disclose a first partial VCO connected to a second VCO. The Examiner then asserts the Iwasaki, and in particular FIG. 8 of Iwasaki, teaches an integrated transceiver on a chip containing inputs for an external VCO and an external VCO and that it would have been obvious to one of ordinary skill in the art to incorporate the external VCO of Iwasaki into the bimodal power data link transceiver of the BlueChip Manual in view of Hareyama. Applicants respectfully disagree.

Col. 5, lines 46-65 of Iwasaki states the following:

> FIG. 8 is a perspective view seeing through another rough structural embodiment of the thin IC card according to this invention, in which reference numeral 1 is a plate type IC module. This plate type IC module 1 includes a semiconductor chip (IC chip) having at least memory and CPU functions and having its one side sealed or molded with a resin, and flat type externally connecting terminals 1a which have their one end connected to the input/output terminals of the semiconductor chip and the other end led and exposed to a non-resin sealed or molded side. Reference numeral 2 is a card-like support which is configured such that the plate type IC module 1 can be attached or removed freely. More specifically, the card-like support 2 includes therein a required circuit wiring (not shown), an antenna 2a for sending and receiving a signal without contacting, an ***oscillator 2c*** for specifying a frequency and a power supply battery 2b, and has a fitting section for fitting the plate type IC module 1 therein with the surface of the externally connecting terminals 1a exposed to be substantially flush with the surface of the card.

Col. 5, lines 46-65 of Iwasaki. The oscillator 2c in Iwasaki is not disclosed as a voltage controlled oscillator. Even assuming for sake of argument that Iwasaki discloses a "voltage controlled oscillator" (which Applicants respectfully submit is not true), Applicants further submit that the Examiner has not established a *prima facie* case of obviousness. As stated in M.P.E.P. §2142:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

M.P.E.P. §2142 (emphasis in original). Applicants respectfully submit that there is no suggestion or motivation to combine the BlueChip Manual (and Hareyama) and Iwasaki. The BlueChip Manual explicitly shows a VCO: see page 1 ("The VCO is a Colpitts oscillator and needs an external resonator and varactor") and FIG. 1 (page 3) of the BlueChip Manual. It is submitted that one skilled in the art would not add a second VCO (e.g., as the Examiner asserts Iwasaki discloses) to the BlueChip Manual, which already has a first VCO. The resultant system would then have two VCOs coupled to each other, whereas only one VCO

would suffice, thereby militating against one skilled in the art adding a second VCO to an IC having a first VCO. The Court of Appeals for the Federal Circuit has stated the following:

> To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that ***the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed.***

In re Rouffet, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) (emphasis added). Applicants outline an exemplary problem as follows:

> In addition, because the many users in a combat environment crowd the electromagnetic spectrum, communications with the landmine must be within a certain predefined range, such as below 200 MHz.
>
> Thus, the above suggests a need for a transceiver having low power requirements. Such a low power transceiver may be fabricated through an Application Specific Integrated Circuit (ASIC). Yet, ASICs, custom made integrated circuits, are expensive and generally cost prohibitive due to their relatively limited production runs. On the other hand, commercial transceivers having low power consumption generally fall into the very high frequency range category, on the order of giga-hertz, well above the 200 MHz operating region of a landmine, and/or fail to have enough power to operate in a burst transmission mode.

Page 2, lines 12-28 of Applicants' specification. It must be pointed out that none of the cited references states that there are problems with the transceiver IC or the use thereof disclosed in the BlueChip Manual. Instead, it was the Applicants who discovered that a reasonable solution to the above-described problems was to operate a transceiver IC at a frequency at which the transceiver IC was not originally intended. Therefore, the Examiner is taking the knowledge of the disclosed invention into account when combining the BlueChip Manual, Hareyama, and Iwasaki, as there is no suggestion in these references of the problem solved by the Applicants, or of the solution presented by Applicants, and there is no motivation to combine these references.

Further, Applicants state the following:

> It will be appreciated that a novel feature of the present invention allows commercial off the shelf transceiver ICs to be adapted to applications not originally intended by the IC manufacturer. For example, the aforementioned 418UHF transceiver is designed to operate at a minimum frequency of 300 MHz. ***However, features of the present invention in the preferred embodiment adapt the IC to operate well below the specified frequency*** and yet maintain the IC's desirable operating characteristics. In addition, ***the remnants of the IC's internal VCO may then be utilized for other functions not originally anticipated by the manufacturer.*** In the preferred embodiment ***the partial VCO*** within the 418 UHF IC is utilized as an emitter follower circuit or buffer. In alternate embodiments the remnants may be utilized as filters. As noted, features of the present invention permit the IC to be used in applications not originally contemplated by its manufacturer.

Page 7, lines 8-23 of Applicants' specification (emphases added). As described above, it was Applicants who determined that providing another VCO outside the IC allows the BC418 UHF transceiver to operate outside the minimum design frequency of 300 MHz and allows the IC's internal VCO to be utilized for other functions. Thus, providing a VCO outside the IC is not something that the manufacturer intended or one skilled in the art would create based on a combination of the BlueChip Manual, Hareyama, and Iwasaki, but is instead something the inventors have determined is useful.

Consequently, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness based on the (invalid) combination of the BlueChip Manual, Hareyama, and Iwasaki. Therefore, independent claims 5, 10, and 20 are patentable over the BlueChip Manual, Hareyama, and Iwasaki for at least the reasons given above.

Because independent claims 5, 10, and 20 are patentable, their respective dependent claims 6, 7, 9, 10, 12, 18, 26-28, are patentable for at least the reasons given above.

It should be noted that newly added claim 29 contains subject matter similar to the subject matter in claims 5, 10, and 20, and therefore independent claim 29 is patentable

for at least the reasons given above with respect to independent claim 5. Because independent claim 29 is patentable, its dependent claims 30-31 are also patentable.

With regard to the rejections in (2)-(5) above, because independent claims 5, 10, and 20 are patentable, their respective dependent claims 8, 11, 13-17, 19, and 23-25 are patentable for at least the reasons given above.

Furthermore, Applicants have added dependent claim 25, which recites "A bimodal power data link transceiver device as in claim 5, wherein the transceiver IC is configured to operate at and above a first frequency and wherein the second VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency." (See, e.g., page 7, lines 7-16 of Applicants' specification: "the aforementioned 418UHF transceiver is designed to operate at a minimum frequency of 300 MHz. However, features of the present invention in the preferred embodiment adapt the IC to operate well below the specified frequency".) There is no disclosure in any of the cited references of a transceiver IC configured to operate at and above first frequency and having a second VCO coupled to a first partial VCO, wherein the second VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency. Therefore, dependent claim 26 is patentable over the cited art. Because dependent claims 27 and 28 recite similar subject matter, these claims are also patentable.

Newly added independent claim 29 also contains subject matter similar to the subject matter in claim 26. For instance, independent claim 29 recites "a transceiver integrated circuit (IC) configured to operate at and above a first frequency" and "a second voltage controlled oscillator (VCO) coupled to the partial first VCO [in the transceiver IC], wherein the second VCO is configured to operate the transceiver IC at a second frequency smaller than the first frequency". Applicants can find no disclosure or implication of this subject matter in any of the cited art and therefore independent claim 29 is patentable over the cited art.

Dependent claim 31 recites "The device of claim 29, wherein the first frequency is 300 megahertz (MHz) and the second frequency is 200 MHz." See, e.g., page 7, line 4 to page 8, line 13 of Applicants' specification. There is no disclosure in any of the cited references of a transceiver IC configured to operate at and above 300 MHz and having a first partial VCO coupled to a second VCO that operates the transceiver IC at 200 MHz. Consequently, dependent claim 31 is patentable over the cited references.

Based on the foregoing arguments, it should be apparent that claims 5-31 are thus allowable over the references cited by the Examiner, and the Examiner is respectfully requested to reconsider and remove the rejections.